AMENDMENTS TO THE DRAWINGS:

Please substitute the attached replacement sheets for Figures 20, 21, 22, and 23 as presented in the replacement drawing sheets filed April 9, 2007. Annotated sheets showing changes to Figures 21 and 22 are also attached.

REMARKS

Favorable reconsideration of the application, as amended, is respectfully requested.

The objection to the drawings has been appropriately addressed. Withdrawal of the rejection is respectfully requested.

By this Amendment, independent Claim 11 has been amended for clarity, and independent Claims 16 and 18 have been amended to recite certain distinctive features of Applicants' invention with greater particularity. Dependent Claims 12-15 and 17 have also been amended for clarity, and new Claim 20 has been added. In amending Claims 11 and 15 for clarity, the objection[1] and the rejection under 35 U.S.C. § 112, second paragraph have been appropriately addressed. Claims 1-10 were previously cancelled. Accordingly, Claims 11-20 are pending, with Claims 11, 16, and 18 being independent.

Turning to the merits, Claims 11 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kengeri in view of Lines; and Claims 13-16, 18, and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kengeri and Lines, further in view of Lines-2.

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[1] Applicants presume that the claim objection was intended to be directed to Claim 11 instead of cancelled Claim 1.

Turning first to the rejection of independent Claims 16 and 18, without acceding to the rejection, these claims have been amended, as noted above.

Independent Claim 16 now recites that the comparator circuit of each memory cell comprises a first MOS transistor and a second MOS transistor connected serially to form a first current path between associated ones of first and second match lines, and a third MOS transistor and a fourth MOS transistor connected serially to form a second current path. Claim 16 further recites that for each first MOS transistor and each third MOS transistor, one of a source electrode and a drain electrode is connected to the associated first match line through a first contact having a lower surface contacting said one source and drain electrode and an upper surface contacted with the first match line, and for each second MOS transistor and each fourth MOS transistor, one of a source electrode and a drain electrode is connected to the associated second match line through a second contact having a lower surface contacting said one source and drain electrode and an upper surface contacting the associated second match line. The lower surface of the first contact is smaller than the upper surface of the first contact, and the lower surface of the second contact is smaller than the upper surface of the second contact.

Kengeri, Lines, and Lines-2 fail to teach or suggest the arrangements of the MOS transistors and the contacts, as well as the sizes of the contact surfaces, as particularly recited in Claim 16.

Accordingly, Claim 16 (and its dependents) is allowable.

As to Claim 18, as now set forth therein, a semiconductor integrated circuit device comprises a plurality of the first match lines, a plurality of search line pairs intersecting the plurality of first match lines, a plurality of bit line pairs arranged parallel to the plurality of search line pairs, and a plurality of memory cells arranged at intersecting points of the plurality of first match lines with associated search line pairs. Claim 18 also now recites that a voltage supplied to the plurality of bit lines pairs varies between a first voltage and a second voltage lower than the first voltage, a voltage supplied to the plurality of search line pairs varies between a third voltage and a fourth voltage lower than the third voltage, and the first voltage is larger than the third voltage.

It is apparent that the collective disclosures of Kengeri, Lines, and Lines-2 fail to teach or suggest at least the foregoing. Therefore, Claim 18 distinguishes

patentably from the collective disclosures of those references and is allowable.

Regarding independent Claim 11, Applicants respectfully traverse the rejection for the reasons discussed below.

Applicants' invention as set forth in Claim 11 is directed to a semiconductor integrated circuit device of a precharge type, in which first and second match lines are precharged, and each second match line is put in a floating state when an associated comparator circuit performs a comparison operation (hereinafter referred to as a "both-precharge-type" semiconductor integrated circuit device). The both-precharge-type semiconductor integrated circuit device provides for low power consumption, but has a problem in that it is susceptible to the influence of noise caused by coupling capacitances between wires associated with search lines. This problem adversely affects device performance.

The inventors of the present invention have discovered a way to overcome the foregoing problem. In particular, the inventors have found that by configuring comparator circuits of memory cells such that MOS transistors of a pair have respective gates connected to associated ones of search lines of a search line pair, and such that each MOS transistor has one of a source and a drain electrode

connected to a first match line associated therewith, it is possible significantly to reduce the influence of noise.

Kengeri is directed to a content addressable memory having a comparator circuit region 110, and which limits its match line voltage swing while not causing significant speed degradation. Kengeri, abstract. However, Kengeri fails to disclose the above-discussed problem recognized by Applicants. Lines' Figure 2 and associated text are directed to a ternary DCAM cell circuit of a type in which matchline ML is precharged, and in which a matchline discharge current is controlled by a current limiting device connected to line ML_VSS and placed in the pitch of each matchline. *See* Lines, Figure 2; Section 3.1. Lines evidently is not directed to a both-precharge-type semiconductor integrated circuit device. Moreover, Lines does not address the problem of the influence of noise caused by coupling capacitances between wires associated with search lines in such a device. Absent any recognition of the "noise" problem identified by the inventors of the present application, one skilled in the art would not resort to the teachings of Lines (which are not related to a both-precharge-type semiconductor integrated circuit device) as a basis to modify Kengeri's comparator circuit region to solve a problem which Kengeri also fails to disclose.

The proposed combination of Kengeri and Lines is therefore inappropriate, and the rejection of Applicants' Claim 11 is untenable and should be withdrawn accordingly.

For the reasons presented above, Applicants respectfully submit that the claims are allowable.

A Notice of Allowance is respectfully solicited.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (XA-10573) any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

By: /Patrick L. Miller/
Mitchell W. Shapiro
Reg. No. 31,568

Patrick L. Miller
Reg. No. 57,502

Miles & Stockbridge, P.C.
1751 Pinnacle Drive
Suite 500
McLean, Virginia 22102-3833
(703) 610-8652

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